Exhibits for Paper #7

USPTO #6 in Reexam 3495

1/25/95

Exhibit A

Exhibit A

UNITED STATES DEPARTMENT OF COMMERCE
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CONTROL NUMBER	FILING DATE	PATENT UNDER REEXAMINATION	ATTORNEY DOCKET NO.
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~~CARROLL, J~~	
ART UNIT	**PAPER NUMBER**
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DATE MAILED:	01/25/95

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OSGS FILE No. BSM1/0125 ERQ 004
DATES 25 Mar 95 SHW
PATENTS ORDERED

JAN 27 1995
OK TO FILE

OFFICE ACTION IN REEXAMINATION

☐ Responsive to the communication(s) filed on ______________. ☐ This action is made FINAL.

A shortened statutory period for response to this action is set to expire 2 (TWO) month(s) from the date of this letter. Failure to respond within the period for response will cause termination of the proceeding and issuance of a reexamination certificate in accordance with this action. 37 CFR 1.550(d). EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).

PART I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. [XX] Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Citation, PTO-1449.
3. ☐ Notice of Informal Patent Drawing, PTO-948.
4. ☐ ______________.

PART II SUMMARY OF ACTION:

1a. [XX] Claims 1 to 14 are subject to reexamination.

1b. ☐ Claims ______________ are not subject to reexamination.

2. ☐ Claims ______________ have been cancelled.

3. ☐ Claims ______________ are confirmed.

4. ☐ Claims ______________ are patentable.

5. [XX] Claims 1 to 14 are rejected.

6. ☐ Claims ______________ are objected to.

7. ☐ The formal drawings filed on ______________ are acceptable.

8. ☐ The drawing correction request filed on ______________ is ☐ approved, ☐ disapproved.

9. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received, ☐ not been received, ☐ been filed in Serial No. ______________ filed on ______________.

10. ☐ Since the proceeding appears to be in condition for issuance of a reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 435 O.G. 213.

11. ☐ Other

cc: Requester

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action.

> "A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> "Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person."

The Takakuwa Reference

Claims 7, 8 and 14 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Reference AK, considered with Okabe et al. '878, Reference AL provided by the Requester. With the embodiment shown in amended Figure 4, reproduced as Figure A, infra, Takakuwa teaches a discrete metal oxide silicon field effect transistor (MOSFET) comprising:

> a P-type base region (18) accommodating an N-plus-type source region (12s) and a channel region between the source region and a lightly doped major body wafer portion (10), whereby each of the source and channel regions is an annulus, evidently

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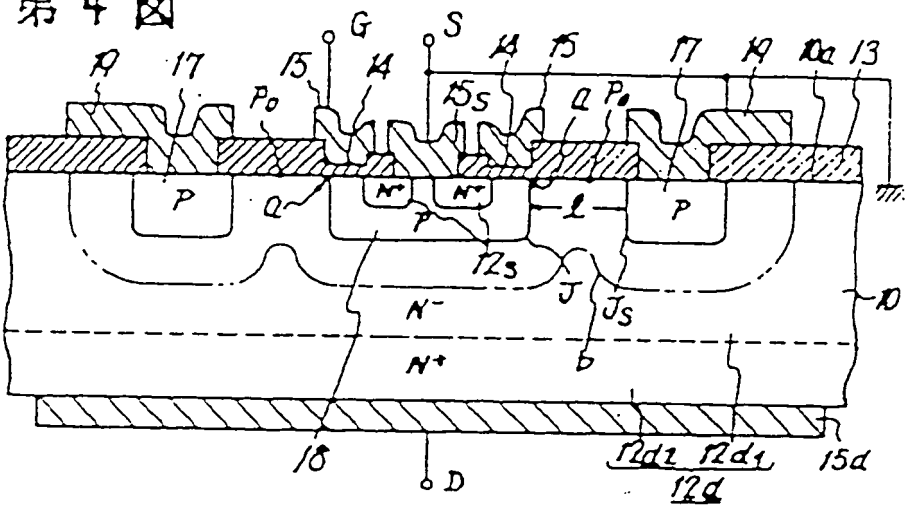

Figure A (Takakuwa Discrete MOSFET
(Reference AK

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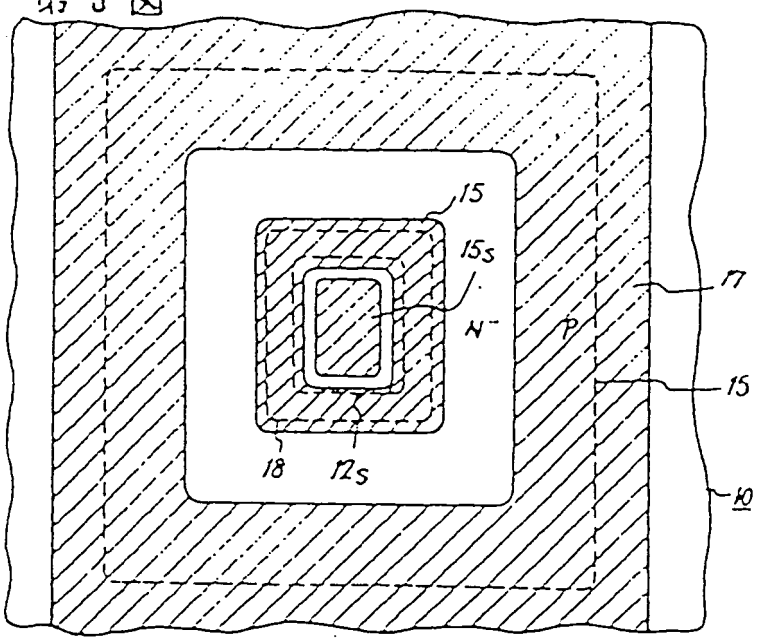

Figure B (Takakuwa Discrete MOSFET
(Reference AK

from Figure 3, reproduced as Figure B, supra;

an N-plus-type drain conductive region (12d2) electrically coupled to drain electrode (15d);

an insulated gate electrode means (15) formed on the channel annulus; and

a source electrode means (15s) electrically contacting the source annulus.

In addition to the discrete MOS transistor embodiment, supra, Takakuwa envisaged an alternative embodiment whereby one forms a "mesh pattern" for base region (18), evidently from the sentence spanning McElroy translation pages 6 and 7. To determine a meaning that one would have ascribed to the "mesh pattern" envisaged by Takakuwa, we find in Okabe et al. '878 sufficient evidence to

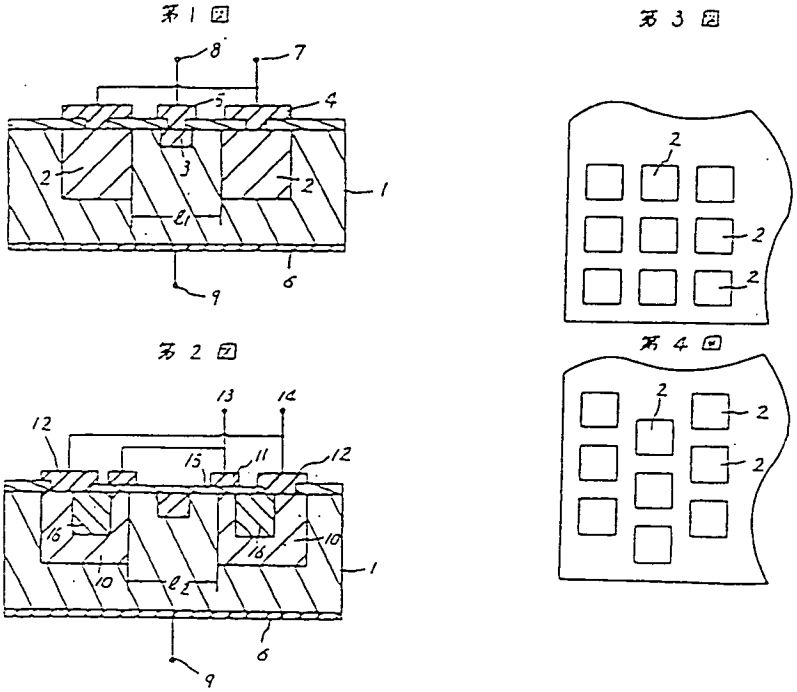

Figure C (Okabe et al. '878 JFET
(and MOSFET Arrays
(Reference AL

conclude that one would have viewed each of the arrays of Figures 3 and 4, reproduced as Figure C, infra, as constituting a mesh pattern whereby Okabe et al. '878 expected to accordingly distribute P-type gate regions (2) of the vertical junction gate field effect transistor (JFET) embodiment illustrated in Figure 1 therein. Okabe et al. '878 analogously expected to accordingly distribute P-type base regions (10) of the vertical MOSFET embodiment illustrated in Figure 2 therein. We thus further conclude it to have been obvious for one to have accordingly construed the

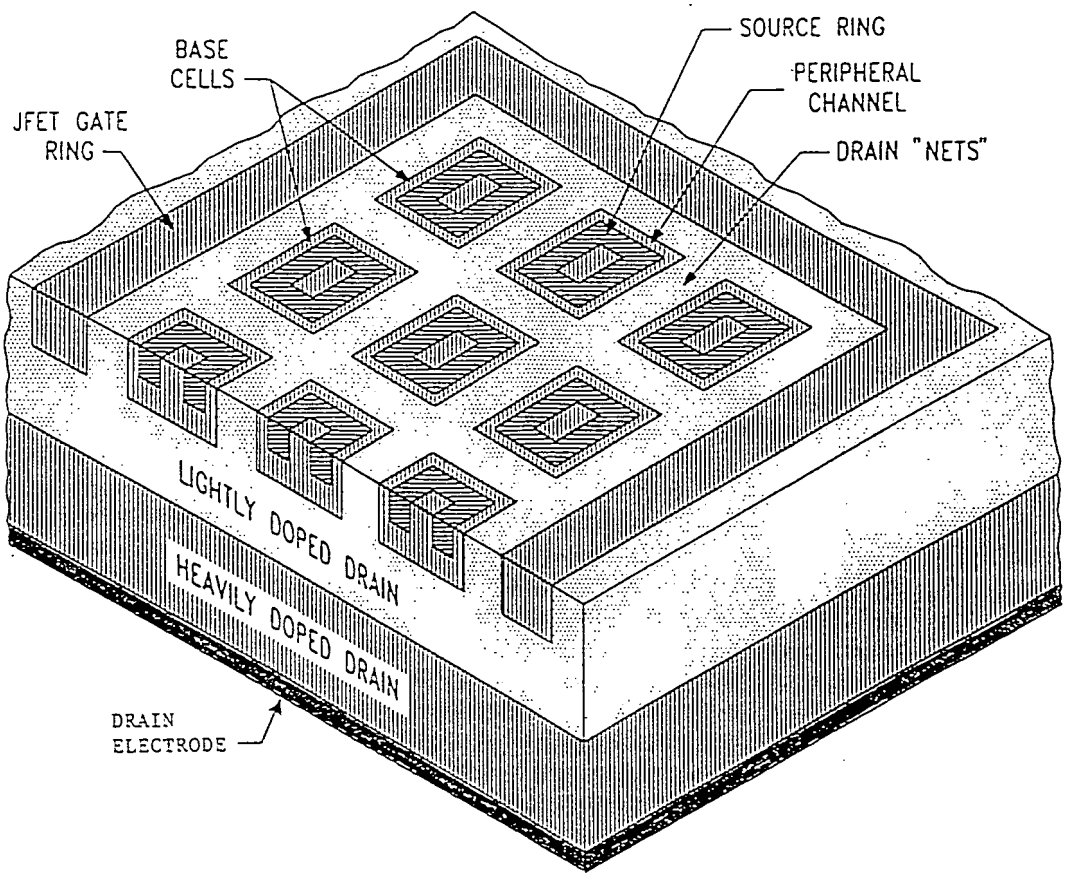

Figure D (Obvious Takakuwa
(MOSFET Array

meaning of "mesh pattern" and to have distributed in a mesh pattern a plurality of Takakuwa base regions (18), as clearly and unambiguously envisaged by Takakuwa, to render thereby an obvious Takakuwa MOSFET array illustrated with Figure D, supra. One readily finds therein a plurality of cellular, polygonal, and identical base regions with each identical polygonal base region accommodating a polygonal source annulus. One further finds that a continuous and uninterrupted common conductive drain mesh region separates one polygonal base region from another.

As an aside, we obtained another English translation of the Okabe et al. '878 document, Reference R presently provided, because we found irreconcilable differences between the available translations. In the Morikami translation, for example, we find on page 2 reference to "rectangular structures" whereas the Liu translation characterizes instead as "plane construction" and "vertical structure". In this example we find the USPTO translation resolves in favor of the Liu translation evidently with a "vertical structure" and a "vertical" field effect transistor.

Claims 3, 5/3 and 13 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa and Okabe et al. '878 as applied supra, but further considered with the Yoshida et al. IEEE article and the Lisiak et al. article, References AO and AQ provided by the Requester. Evidently from the first paragraph on McElroy translation page 7, Takakuwa expected to form a mesh gate electrode (15) in an alternative. To determine a meaning that one would have ascribed to a mesh gate electrode, we find that Yoshida et al. IEEE teaches a meshed gate structure constituted with polysilicon material, especially with Figures 1(a) and 1(b)

reproduced as Figure E, infra. We thus conclude that one would have accordingly incorporated a meshed gate structure within the obvious Takakuwa MOSFET array alternative. Takakuwa does not particularly teach a source electrode structure for the alternative embodiment. We conclude therefrom that any particular source electrode structure usually used in a mesh-gate, mesh-base MOSFET array would have been obvious, i.e., the source electrode single sheet structure envisaged by Yoshida et al. IEEE. We thus

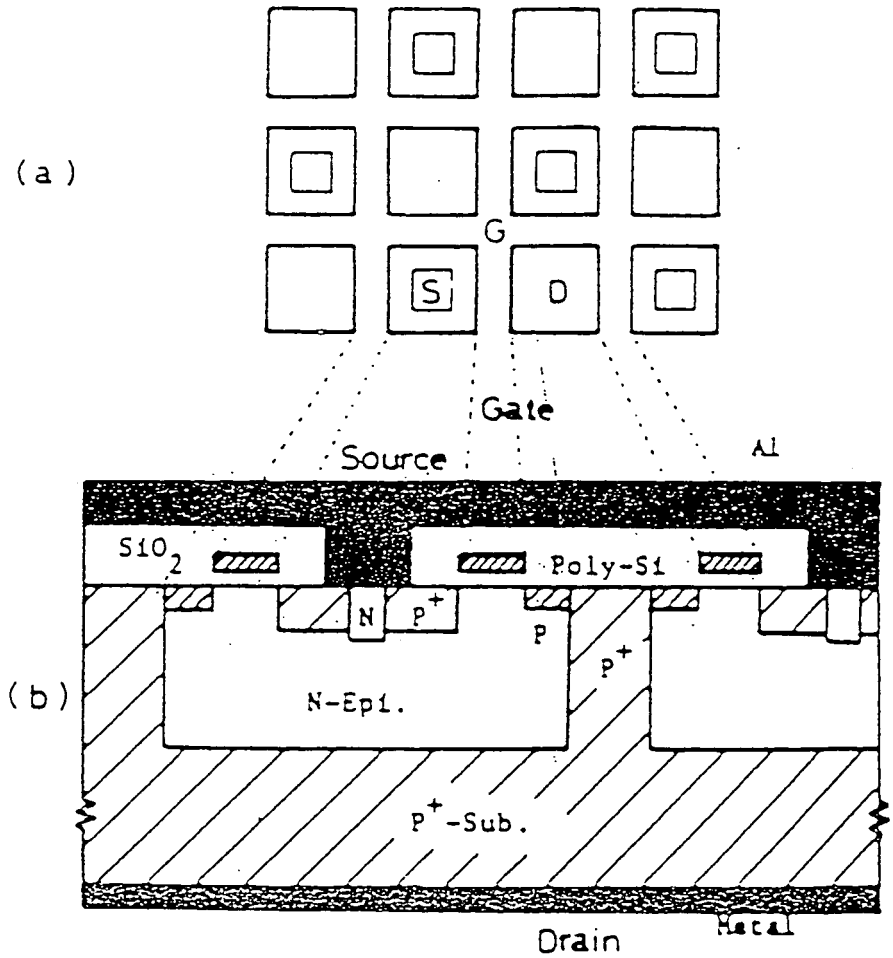

Figure E (Yoshida et al. IEEE MOSFET
(Array with Meshed Gate and
(Sheet Source Electrode
(Reference AO

further conclude it to have been obvious for one to have accordingly applied the meshed-gate structure and single sheet source electrode structure of Yoshida et al. IEEE to the obvious Takakuwa MOSFET array alternative shown with Figure D, supra, to render thereby a fully contacted, Takakuwa MOSFET array structure illustrated with Figure F, infra, appropriately incorporating the meshed-gate and single sheet source electrode structure of Yoshida et al. IEEE. Lisiak et al. render their perception of

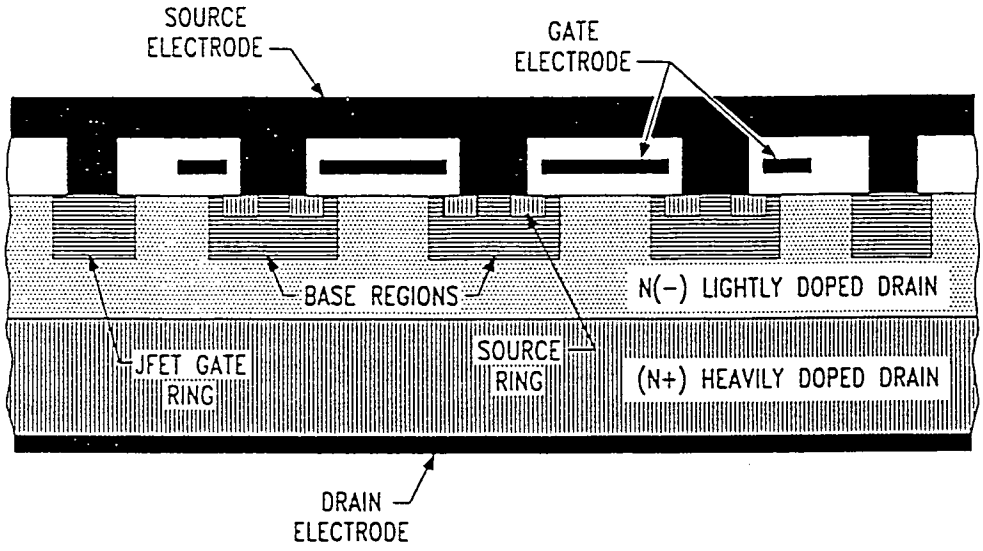

Figure F (Obvious Takakuwa MOSFET
(Array Incorporating
(Meshed-Gate and Sheet
(Source Electrode of
(Yoshida et al. IEEE

the Yoshida et al. IEEE MOSFET array with Figure 7(b) therein showing a lateral MOSFET cell repeat distance of about 44 microns. We thus still further conclude it to have been obvious for one to have realized that the Yoshida et al. IEEE MOSFET array as perceived by Lisiak et al. is comprised of more than one thousand MOSFET cells within a two-lateral-inch distance. Simi-

larly, one may accordingly comprise the obvious Takakuwa MOSFET array of Figure F, supra, with more than one thousand MOSFET cells within a two-lateral-inch distance.

In re Claim 13, Lisiak et al. discuss as advantageous options MOSFET cell arrays having lateral MOSFET cell repeat distances other and less than 44 microns, i.e., 40 microns, 25 microns and 10 microns. We thus moreover conclude it to have been obvious for one to have accordingly comprised the obvious Takakuwa MOSFET array of Figure F, with a MOSFET cell repeat distance as small as 25 microns, about one mil, and as small as 10 microns, about 0.4 mil.

In re Claim 3, Takakuwa characterizes N-minus-type layer (7) of the DMOS transistor embodiment of Figure 2 as an epitaxial layer. Takakuwa does not similarly characterize comparable N-minus-type layer (10) of the discrete MOSFET embodiment shown with Figure A, supra. We conclude therefrom that Takakuwa expected one to have realized that comparable layer (10) may be constituted as an epitaxial layer.

Claims 1 and 5/1 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE and Lisiak et al. as applied supra, but further considered with Fukuta, Reference AA provided by the Requester, teaching a plurality of MOSFET array embodiments comprising a regular square array pattern of source and drain regions as illustratively shown with Figures 1 and 2A therein. Evidently from the paragraph beginning on line 47 of column 4 and Figure 3, reproduced as Figure G, infra, Fukuta envisaged at least an alternative, closely

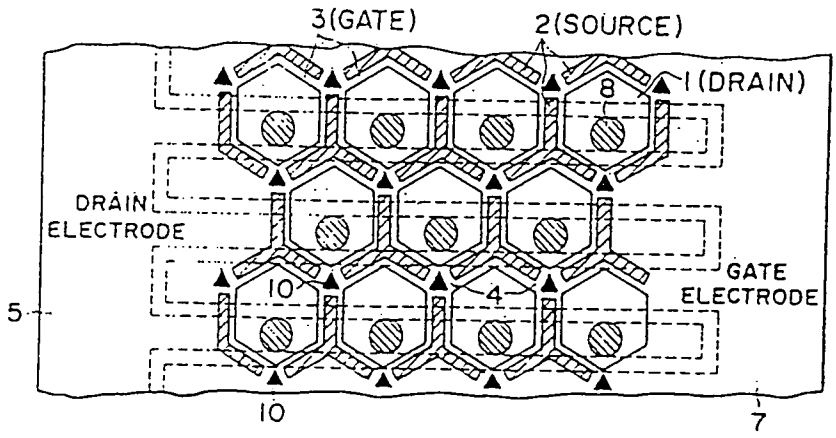

Figure G (Fukuta Hexagonal MOSFET
(Array Reference AA

packed, hexagonal array pattern. We thus find in Fukuta sufficient evidence to conclude that one who practiced in the MOSFET array art at the time of Takakuwa would have similarly and readily envisaged a closely packed, hexagonal MOSFET array. We thus further conclude that the MOSFET mesh arrays, clearly and unambiguously envisaged by Takakuwa, would have included closely packed, hexagonal MOSFET arrays as evidenced by Fukuta. Similarly as shown with Figure D, supra, an obvious Takakuwa MOSFET array would have comprised a hexagonally close-packed array of hexagonal base regions separated from one another by a continuous, uninterrupted and hexagonal, common conductive drain mesh, whereby each hexagonal base region accommodates a hexagonal source annulus.

Claim 4 is rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE,

Lisiak et al. and Fukuta, as accordingly applied to Claims 1 and 3, supra, but further considered with the Krishna article, Reference AP provided by the Requester. Krishna reports results from an analysis aimed at obtaining a better understanding of secondary breakdown failure mode in high voltage lateral and vertical MOS transistors. Krishna found it desirable to provide space between base regions in a vertical MOSFET array

"of the order of microns",

excerpted from the last paragraph on page 877. Krishna in Figure 1b therein posed a range between about one and ten microns. Presuming that about 15 microns, about 0.6 mil, falls within the scope "of the order of microns" envisaged by Krishna, we conclude it to have been obvious for one to have accordingly spaced from one another the base regions of the obvious Takakuwa MOSFET array of Figure F, supra, so as to achieve desirable, secondary breakdown characteristics as found by Krishna.

Claims 2, 6, 9 and 10 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta as applied supra to Claims 1, 3, 7 and 8, but further considered with Lidow et al. '286, '666, '759 and '699, References AF, AG, AH and AI, respectively provided by the Requester. Lidow et al. teach the prudent advantages of providing a lattice material of Claims 1 and 3, and a common conductive region of Claims 7 and 8 comprising particular impurity concentration and depth relationships as claimed to desirably reduce the on-resistance characteristic. We thus conclude it to have been desirably prudent and obvious thereby for one to have accordingly reduced the on-resistance characteristic of the obvious Takakuwa MOSFET arrays.

Claims 11 and 12 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as accordingly applied supra to Claims 1, 3, 7 and 8, but further considered with Ishitani, Reference AB, corroborated by Lidow et al. '286, '666, '759 and '699, References AF, AG, AH and AI, respectively, Sakai '688 of record in Reexamination Control Number 90/002,478 (Reexam 2478), and presently provided Tihanyi et al., Plummer et al., Scharf et al. and Pocha et al., References A, S, T and U, respectively. Ishitani discloses a MOSFET array device illustrated therein with Figure 4I and reproduced with Figure H, infra, that is similar to

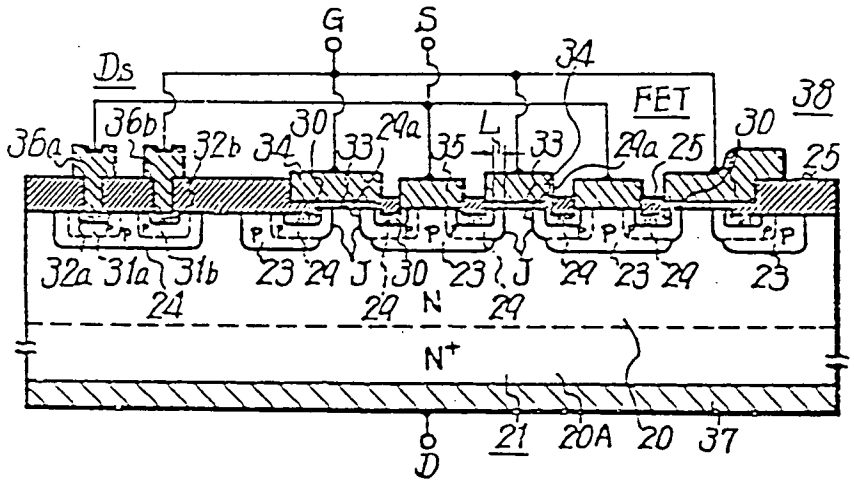

Figure H (Ishitani MOSFET Array with
(Deepened Base Regions (23)
(Reference AB

the obvious Takakuwa MOSFET array device shown with Figure D, supra. Ishitani deepens base region (29) beneath source contacts (35) to form frame region (23) of larger thickness so that

> "no possibility that the short-circuit between the source and drain regions occurs by the migration of the source electrode 35",

excerpted from lines 7, 8 and 9 of column 7. Each of the corroborating MOSFET references includes a base region comparable to the deeper base frame region (23) of Ishitani but without the rationale as expressed by Ishitani. It thus becomes evident and obvious thereby that the rationale as disclosed by Ishitani constitutes common knowledge and common sense possessed by those of ordinary skill who practice in the MOSFET art. We thus conclude it to have been obvious for one to have exercised common knowledge and common sense and accordingly deepen base regions beneath source contacts in the obvious Takakuwa MOSFET array of

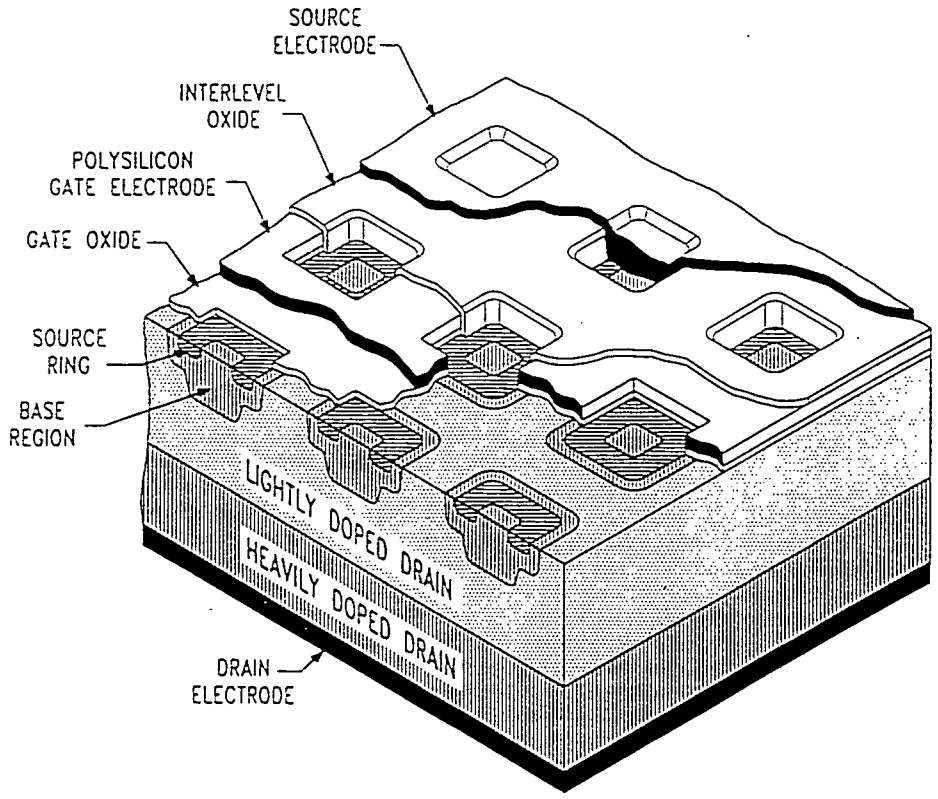

Figure I (Obvious Takakuwa MOSFET
(Array Incorporating Source
(and Gate Electrodes of
(Yoshida et al. IEEE and
(Deepened Base regions
(Similar to Ishitani

Figure F, supra, and obtain thereby the obvious Takakuwa MOSFET array shown with Figure I, supra, appropriately incorporating sheet source and polysilicon gate electrodes of Yohsida et al. IEEE and deepened base regions similar to Ishitani.

The Hendrickson Patent

Claims 3, 5/3, 7, 8 and 14 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Reference AE provided by the Requester, considered with presently cited and provided Lee and Declercq et al., References R' and S', respectively, but further considered with Ishitani, Reference AB provided by the Requester. Hendrickson expected to form a vertical V-gate MOSFET hexagonal array evidently from Figure 14, reproduced as Figure J, infra, showing a cross-section taken from the plan layout of Figure 7 therein, whereby the GATE electrode is formed in an aniso-

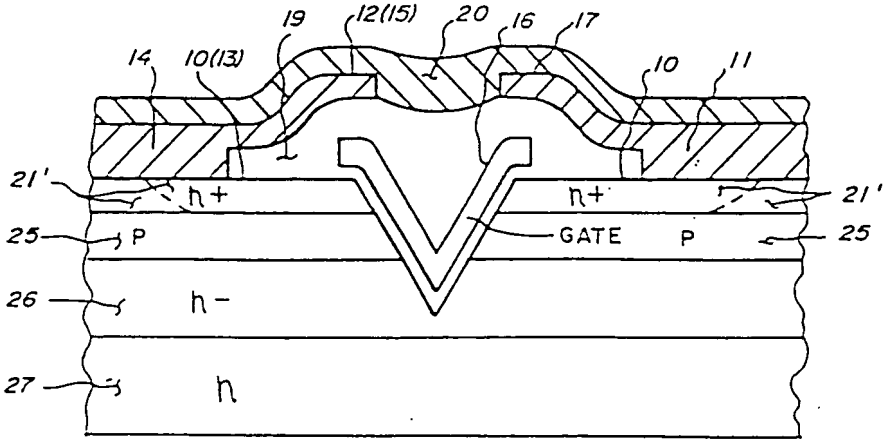

Figure J (Hendrickson MOSFET Array
(Reference AE

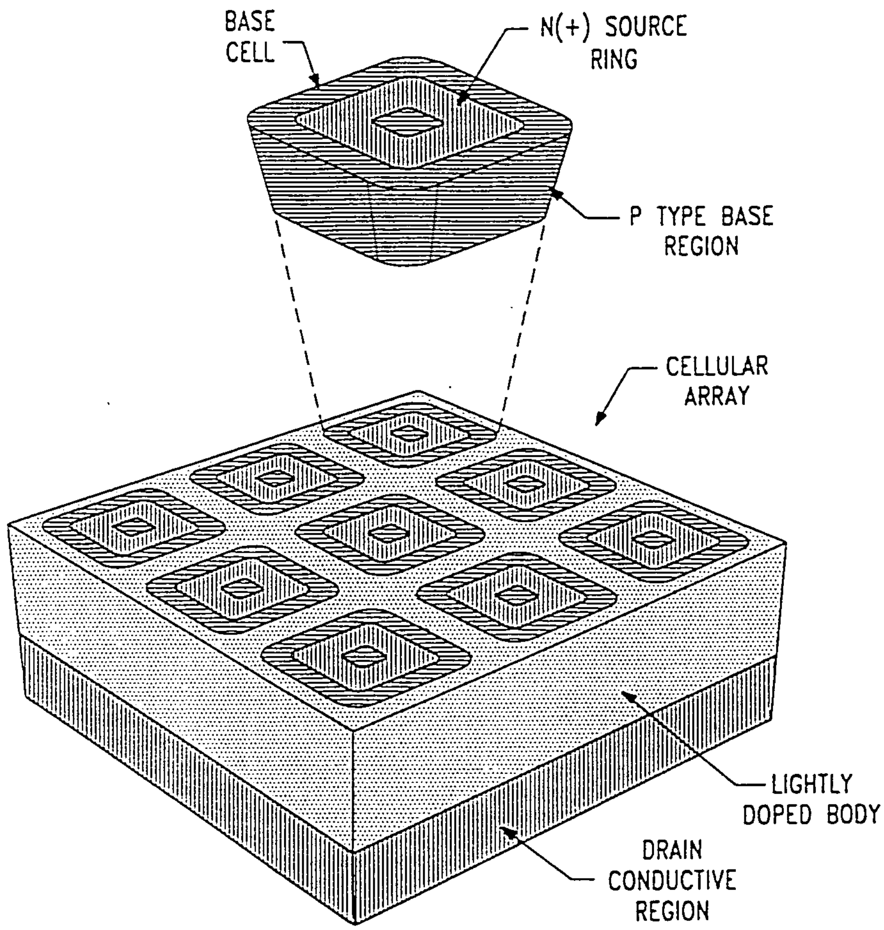

Figure K (Obvious Hendrickson Planar
(MOSFET Array Void of The
(Undesirable V-Groove as
(Characterized by Ishitani

One readily discerns therein an array of identical polygonal base regions, symmetrically disposed and equally spaced from one another by a continuous and uninterrupted polygonal lattice of N-minus-type drain material.

In re Claims 7 and 8, Ishitani anticipated coupling drain electrode (37) to N-plus-type drain conductive layer (21). We

thus conclude it to have been obvious for one to have accordingly coupled a comparable drain electrode to N-type drain conductive layer (27) of Hendrickson.

In re Claim 3, Hendrickson anticipated constituting N-minus-type wafer portion (26) as an epitaxial layer, evidently from the sentence beginning on line 35 of column 13; Hendrickson anticipated constituting gate electrode runs with polysilicon material, evidently from the sentence beginning on line 34 of column 10; and Hendrickson anticipated forming more than a thousand parallel-connected MOSFETs, evidently from the sentence beginning on line 9 of column 10.

In re Claims 5/3 and 14, Hendrickson anticipated using N-plus-type source regions (21'), P-type base regions (25), and an N-minus-type, lightly doped, wafer portion (26), evidently from Figure J, supra.

Claim 13 is rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani, as applied supra, but further considered with the Lisiak et al. article, Reference AQ provided by the Requester, teaching the advantageous option of comprising vertical MOSFET arrays with lateral, MOSFET cell repeat distances of about 40 microns, 25 microns and 10 microns. We thus conclude it to have been recognized as being similarly advantageous and obvious thereby for one to have accordingly comprised the obvious Hendrickson planar vertical MOSFET of Figure K, supra, with a MOSFET cell lateral repeat distance of about 25 microns, i.e., about one mil.

Claim 4/3 is rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani, as applied supra to Claim 3, but further considered with the Lisiak et al. article similarly as discussed supra with respect to Claim 13, but still further considered with the Krishna article, Reference AP provided by the Requester. Krishna reports results from an analysis aimed at obtaining a better understanding of secondary breakdown failure mode in high voltage lateral and vertical MOS transistors. Krishna found it desirable to provide space between base regions in a vertical MOSFET array

"of the order of microns",

excerpted from the last paragraph on page 877. Krishna in Figure 1b therein posed a range between about one and ten microns. Presuming that about 15 microns, about 0.6 mil, falls within the scope "of the order of microns" envisaged by Krishna, we conclude it to have been obvious for one to have accordingly spaced from one another the base regions of the obvious Hendrickson planar MOSFET array of Figure K, supra, so as to achieve desirable secondary breakdown characterisics as found by Krishna.

Claims 6, 9 and 10 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani as applied supra to Claims 3, 7 and 8, but further considered with Lidow et al. '286, '666, '759 and '699, References AF, AG, AH and AI, respectively, provided by the Requester. Lidow et al. teach the prudent advantages of providing a lattice material of Claim 3 and a common conductive region of Claims 7 and 8 comprising particular impurity concentration and depth relationships, as claimed, to desirably reduce the on-resistance characteristic. We thus conclude it to have been desirably prudent and obvious

thereby for one to have accordingly reduced the on-resistance characteristic of the obvious Hendrickson MOSFET arrays.

Claims 11/3, 11/7, 11/8, 12/11/3, 12/11/7 and 12/11/8 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani as applied supra to Claims 3, 7 and 8, but again considered with Ishitani as corroborated by Lidow '286, '666, '759 and '666, References AF, AG, AH and AI, respectively, Sakai '688, of record in Reexam 2478, and presently cited and provided Tihanyi et al., Plummer et al., Scharf et al. and Pocha et al. References A, S, T and U, respectively. Ishitani expected to form deeper base regions (23) shown in Figure H, supra, so that

> "no possibility that the short-circuit between the source and drain regions occurs by the migration of the source electrode 35",

excerpted from lines 7 to 9 of column 7 therein. We thus conclude it to have been obvious for one to have accordingly deepened base regions (25) of Hendrickson beneath source contact (11) (14) so that no possibility that a short-circuit between source (21') and drain (26) regions occurs in the obvious Hendrickson planar MOSFET array. The corroborating evidence as a whole suggests that the Ishitani rationale, excerpted supra from lines 7 to 9 of column 7, constitutes common knowledge and common sense possessed by those of ordinary skill who practice in the semiconductor MOSFET art. We thus conclude it to have been obvious for one to have exercised common knowledge and common sense and accordingly deepen P-type base regions (25) of Hendrickson beneath source contact (11) to optionally allow a more shallow base region to partially underlay N-plus-type source regions (21') of

Hendrickson, as aptly shown by Scharf et al. with Figure 1 therein, reproduced as Figure L, infra.

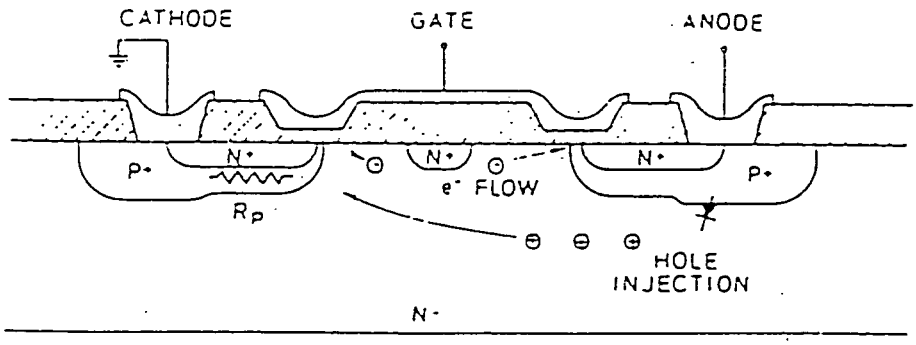

Figure L (Scharf et al. MOSFET Array
(Reference T

Double Patenting Considerations

Present Claims 7, 8 and 14 of US 5,008,725 (Claims 7, 8 and 14 '725) are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of US 4,959,699 (Claim 1 '699) considered further with Takakuwa and Okabe et al. In view of Okabe et al., Takakuwa envisaged a mesh-base MOSFET having a configuration shown with Figure D, supra, that is fully consistent with not only Claims 7, 8 and 14 '725, as established supra, but also fully consistent with the subject matter scoped out by Claim 1 '699. We perforce conclude therefrom that each of Claims 7, 8 and 14 '725 is thereby obvious over Claim 1 '699.

Claims 3, 5/3 and 13 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as be-

ing unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al., Yoshida et al. IEEE, and Lisiak et al. Evidently from considerations of Okabe et al., Yoshida et al. IEEE, and Lisiak et al., Takakuwa envisaged a mesh-base, mesh-gate, and sheet source electrode MOSFET as shown with Figure F, supra, that is fully consistent with not only Claims 3, 5/3 and 13 '725, but also fully consistent with the subject matter scoped out by Claim 1 '699. We thus conclude therefrom that each of Claims 3, 5/3, and 13 '725 is thereby obvious over Claim 1 '699.

Claims 1 and 5/1 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al., Yoshida et al. IEEE, Lisiak et al. and Fukuta. Takakuwa evidently envisaged a mesh-base MOSFET comprising an hexagonally close-packed array of hexagonal base regions separated from one another by a continuous, uninterrupted and hexagonal, common conductive drain mesh, whereby each hexagonal base region accommodates a hexagonal source annulus. Further considering that the Takakuwa device is fully consistent with Claim 1 '699, we conclude that each of Claims 1 and 5/1 '725 is thereby obvious over Claim 1 '699.

Claim 4 '725 is rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al., Fukuta and Krishna making obvious the claimed dimensions within a Takakuwa mesh-base MOSFET. Further considering that the Takakuwa device is fully consistent with Claim 1 '699, we conclude that Claim 4 '725 is thereby obvious over Claim 1 '699.

Claims 2, 6, 9 and 10 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claims 2 and 6 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as essentially discussed supra.

Claims 11 and 12 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 7 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as essentially discussed supra.

The double patenting rejections are based upon judicially established doctrine grounded in public policy, a policy reflected in the statute, so as to prevent an unjustified and improper time-wise extension of the right to exclude as granted by a patent, after In re Sarett, 140 USPQ 474 (CCPA 1964); In re Schneller, 158 USPQ 210 (CCPA 1968); In re White, 160 USPQ 644 (CCPA 1969); In re Thorington, 163 USPQ 644 (CCPA 1969); In re Vogel, 164 USPQ 619 (CCPA 1970); In re Van Oram, 214 USPQ 761 (CCPA 1982); In re Longi, 225 USPQ 645 (Fed. Cir. 1985); and In re Goodman, USPQ 2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer under 37 C.F.R. 1.321(b) would overcome the obviousness-type double patenting rejections provided the conflicting '699 Patent is shown to be commonly owned with the '725 Patent, after 37 C.F.R. 1.78(d).

We reject all Claims.

We set a period for response of two months from the date of this USPTO action.

An inquiry concerning this communication may be directed to Examiner J. Carroll at telephone number 703-308-4926, or to the Group 2500 Receptionist at telephone number 703-308-0956.

Respectfully Submitted.

JAMES J. CARROLL
EXAMINER
ART UNIT 253

JANICE A. HOWELL
DIRECTOR
GROUP 2500